CLAIMS

1. An integrated circuit with a D.C./D.C. voltage regulator comprising at least one power stage provided with at least two transistors and with at least one capacitor connecting a control electrode of the transistor to a reference voltage, a same control stage of the regulator providing a control signal of said transistors, wherein the power stage is formed under a rail that provides of supply signals of the integrated circuit, said rail providing at least two limiting supply voltages coming from the outside of the integrated circuit and at least one voltage regulated by said voltage regulator.

2. The circuit of claim 1, wherein said rail further provides said control signal.

3. The circuit of claim 1, wherein said transistors are formed in an active area underlying two close conductors that provides one of the limiting voltages and of said regulated voltage.

4. The circuit of claim 1, wherein said capacitor is formed straight above a conductor providing a reference voltage corresponding to one of said limiting voltages.

5. The circuit of claim 1, wherein the control electrodes of the transistors are formed of parallel conductive strips arranged perpendicularly to the conductors of said rail.

6. The circuit of claim 1, wherein said voltages are provided in a first metallization level of the integrated circuit.

7. The circuit of claim 1, wherein said control stage is formed in a core of the integrated circuit, around which is arranged said rail in a crown of circuit inputs/outputs.

8. A method for forming at least one power stage of a voltage regulator formed of at least two MOS transistors and of at least one capacitor connecting a control electrode of said transistors to a reference voltage, comprising forming said transistors under a rail that provides supply signals of the integrated circuit, in a crown of

inputs/outputs thereof, said rail providing at least said reference voltage, a regulated voltage provided by the power stages, and a supply voltage thereof.

9. The method of claim 8, wherein said capacitor is formed under said rail.